REMARKS

Claims 29-38 are pending. Of those, claims 29-33 are rejected on double-patenting grounds. Claims 34 and 37-38 are rejected as obvious under 35 U.S.C. § 103(a). Double patenting rejections are traversed in-part and, in-part, overcome by amendment. Obviousness rejections are traversed in-part and, in-part, overcome by amendment. *Finally, with respect to claims 35 and 36, Applicant notes that no basis whatsoever has been provided for rejection and applicant requests an indication of allowability.*

Drawing Informalities

Examiner has objected to certain informalities of Figure 1. A proposed drawing correction submitted herewith adds appropriate legends and identifies high-bandwidth, low-latency communication channels (e.g. the "4 arrow element") using a reference number. The specification has been amended to recite the reference number. Support appears in the specification at least at page 6, lines 15-23. No new matter is added.

Withdrawal of Finality – Substantive Examination of Claims 35-36

As noted above, no basis whatsoever has been provided for rejection of claims 35-36. Applicant requests withdrawal of the prior final rejection, substantive examination of claims 35-36 and an indication of allowability.

Amendment to Place Claims in Better Condition for Appeal

Entry of the claim amendments is respectfully requested. In particular, amendment of claim 33 and cancellation of claims 31-32 serve to focus statutory double patenting issues. Amendment of claim 34 serves to focus on scope and content of the cite art in relation to thread switch control.

Statutory Double Patenting -Rejections under 35 USC §101

Claims 29-32 and 34-38 have been rejected under 35 USC §101 as claiming the same invention as that of claims 1 and 11-12 of prior U.S. Patent No. 6,205,543. Applicants respectfully traverse these rejections.

In rejecting claim 29, Examiner has restated his reasons from prior office action dated July 24, 2002. In particular, Examiner has stated that "Applicants fail to provide any arguments as to why the elements of the rejected claims do not correspond to the elements in the patented claims." Applicants respectfully note that in responding to previous office action, not only did Applicants identify a specific limitation of patented claim 1 not recited in presently rejected claim 29, but also identify a specific legal error, namely failure to provide the literal infringement analysis required to establish a prima facie case for same-invention double patenting (*See* In re Vogel 164 U.S.P.Q. 619 and MPEP § 804). Examiner's statutory double patenting rejection was (and is, now again) properly traversed. Applicant respectfully notes that the proper legal standard for statutory double patenting is identity not correspondence.

Therefore, subject matter of claim 29 differs from that of claim 1 of U.S. Patent No. 6,205,543 in at least the following substantial ways. Claim 29 of the application does not include the limitation requiring that "dirty bit logic" is "`responsive to a context switch by saving storage groups based on the evaluation of the classified destinations`" as recited in claim 1 of the patent. Though of differing scope, claim 33 (as now amended) can be similarly distinguished from patented claim 1 in that no "`[response] to a context switch by saving storage groups based on the evaluation of the classified destinations`" is required by the pending claim. Accordingly, Applicants respectfully submit that claims 29 and 33 and those dependent therefrom are patentably distinguishable from the cited patent and withdrawal of the double patenting rejection is respectfully requested.

Rejections under Non-statutory Obviousness-type Double Patenting

Claim 33 has been rejected under the judicially created doctrine of double patenting over claims 1 and 20 of U.S. Patent No. 6,408,383. Without acquiescing in the propriety of the

rejection, Applicants are willing to submit a terminal disclaimer in compliance with 37 CFR § 1.321(c) once claim 33 is indicated as otherwise allowable.

Rejections under 35 U.S.C. § 103(a)

Claims 34 and 37-38 have been rejected as obvious over U.S. Patent No. 6,470,433 to Emer et al (*Emer*). Applicants have amended to emphasize relation between "the context switch controller" and "dirty bit storage."

In rejecting claim 34, Examiner has effectively discounted the term "context switch controller." In particular, the Examiner assumes that *Emer's* disclosure of a processor including registers with associated valid bits teaches or suggests a context switch controller that employs dirty bits in the way claimed by Applicants. Careful reading of *Emer* makes clear that no such switch controller is disclosed. Indeed, Examiner relies on general background description of thread context switching (col. 1, line 36) in a CPU and improperly mates that description with totally unrelated description of register associated valid bits (col. 5, lines 3-6). Examiner's reliance aside, there is simply no relation, in *Emer*, between thread context switch control and valid bits. Valid bits are employed in *Emer* to signal that an operand of an instruction are available and that the instruction can be issued. Valid bits have nothing at all to do with context switch control.

To emphasize that the claimed context switch controller employs dirty bits, claim 34 has been amended to recite that "operation of the context switch controller is based, at least in part, on state of the dirty bit storage." Claim 34 and those dependent therefrom are all allowable over *Emer* and a notice to that effect is respectfully requested.

In view of the remarks set forth herein, the application and claims therein are believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be amendable to resolution through a telephone interview, the Examiner is requested to telephone the undersigned.

PATENT

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